EENG 443 Digital IC Design - Course Description

Semester	Fall 2017-18	Pre-requisite: EENG 115 and EENG 341	Credit Hrs. : 4
Instructor	Dr. Gürtaç Yemişcioğlu		gurtac.yemiscioglu@emu.edu.tr
Course Web:	http://opencourses.emu.edu.tr/course/view.php?id=369		

CATALOGUE DESCRIPTION:

The fundamental concepts of modern digital VLSI circuit design using CMOS technology with an emphasis on "hands-on" IC design using CAD tools, an overview of CMOS technology, simple and extended circuit models for NMOS and PMOS transistors, combinatorial and sequential logic circuits including transistor level design of logic gates at the device and layout level, digital CMOS IC design flow, hardware Description Languages (VHDL), architectural aspects of a VHDL, synthesised VHDL on physical hardware, chip level design methodologies (full-custom, semi-custom and standard cell) exploration and Alternative low-power logic families.

PREREQUISITE BY TOPIC:

Binary numbers, logic gates, combinational and sequential circuits.

Textbook: S. Brown, Z. Vranesic, Fundamentals of Digital Logic with HDL Design (Third Edition) , Mc-Graw Hill 2009.

REFERENCES:

- V. A. Pedroni, Circuit Design with VHDL, MIT Press 2004.
- R.J. Baker, CMOS Circuit Design, Layout and Simulation 3rd Edition, IEEE Press 2010.
- Rabaey, Digital Integrated Circuits, 2002
- W. Wolf, Modern VLSI Design 4th Edition Prentice Hall, 2009
- D. Clein, CMOS IC Layout Concepts, Methodologies and Tools, 2000

COURSE OBJECTIVE: At the end of this course students will

Learn the design process with an emphasis on hands-on CMOS digital IC design

Have an ability to design digital logic circuit schematics and layouts circuits using appropriate CAD tools and CMOS process.

Have an ability to use a design flow to design complex CMOS digital integrated circuits.

Have an ability to build a cell library to be used in/by other designs/designers.

Have an ability to analyse circuits using both analytical and spice tools.

Have an ability to derive analytical circuit equations to estimate and compute power efficiency of a VLSI design.

Have an ability to code in VHDL and simulate using Modelsim™

Have an ability to design test benches that can prove that a design meet a specification.

Have an ability to synthesise VHD on to hardware using Xilinx tools

Have an ability put together all logical/control units and add the appropriate pads to a layout.

Office Hours: TBA

COURSE OUTLINE & ORGANISATION

WEEK #	DESCRIPTION
1-2	INTRODUCTION TO DIGIAL ICs: Digital Hardware, the evolution of digital circuit design, why design ICs? Types of ICs, the CMOS IC design flow, manufacturing process, introduction to CAD tools.
3-6	DESIGN ENTRY: ASIC Cell Libraries, introduction to VHDL, devices & schematic fundamentals, VHDL data types, operators and attributes, IC design techniques, ASIC design rules.
7	MIDTERM EXAMINATION
8-9	LAYOUT DESIGN: Stick diagrams, introduction to transistor layout, combinational logic gates in CMOS and VHDL, sequential circuits in CMOS and VHDL.
10-12	IC IMPLEMENTATION STRATEGIES and STATE MACHINES: Custom circuit design, digital system design, state machines In VHDL, timing classification of digital systems.
13-14	TESTING ICs, LOGIC BLOCKS AND CAD TOOLS: Testing of logic circuits, arithmetic building blocks, subsystem design, floor planning and packaging ICs, CAD tools.
15	FINAL EXAMINATION

DESIGN COMPONENT:
Engineering Science Credit: 2
Engineering Design Credit: 2

LABORATORY/STUDIO WORKS:
Laboratory sessions are organized in parallel to theoretical study given in classrooms. Students perform at least 10 different experiments and submit designs for evaluation.

GRADING SYSTEM	
Midterm Exam	25%
Quizzes	5%
Lab	25%
Homeworks	15%
Final	30%

NG POLICY:

Students who do not pass the course and fail to attend the lectures regularly may be given the NG grade.

MAKE-UP EXAMINATION POLICY:

Students missing an examination should provide a valid excuse within three days following the examination they missed. No separate make-up exams are administered for midterm and final exams. Re-sit examination is administered as make-up examinations, instead.
Students who fail to attend less than 60% of classes will not be given Make-up examination.